T-46-09-05

Signetics

FAST 74F605 Register

Dual Octal Register (Open Collector)

Product Specification

FAST Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **Open Collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

DESCRIPTION

The 74F605 contains 16 D-type edge triggered flip-flops with commom clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight Open Collector outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the flip-flops on the rising edge of the clock (CP) input, which also controls the Open Collector outputs. The outputs are enabled when CP is High and disabled when CP is Low.

These functions are well-suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	105MHz	85mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F605N
28-Pin Plastic SOL	N74F605D

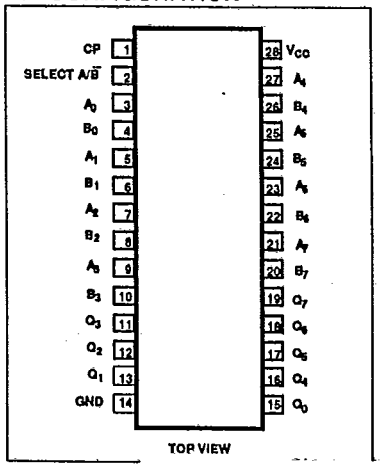
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (active rising edge)	1.0/0.033	20μA/20μA
Q_0-Q_7	Data outputs	OC/40	OC/24mA

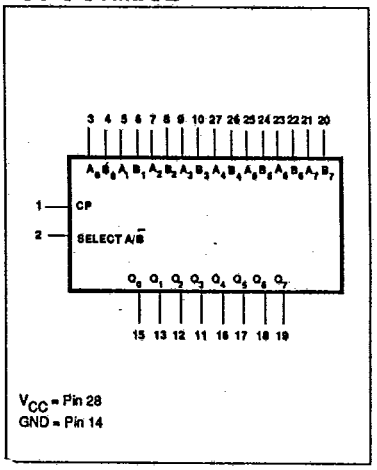
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

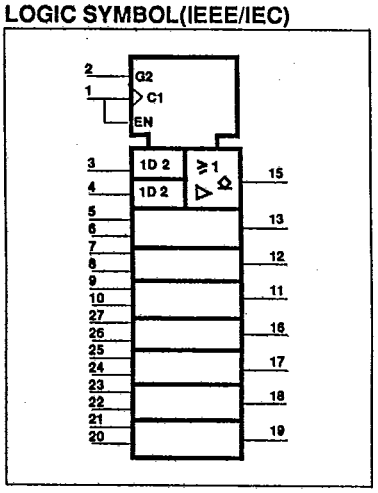
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



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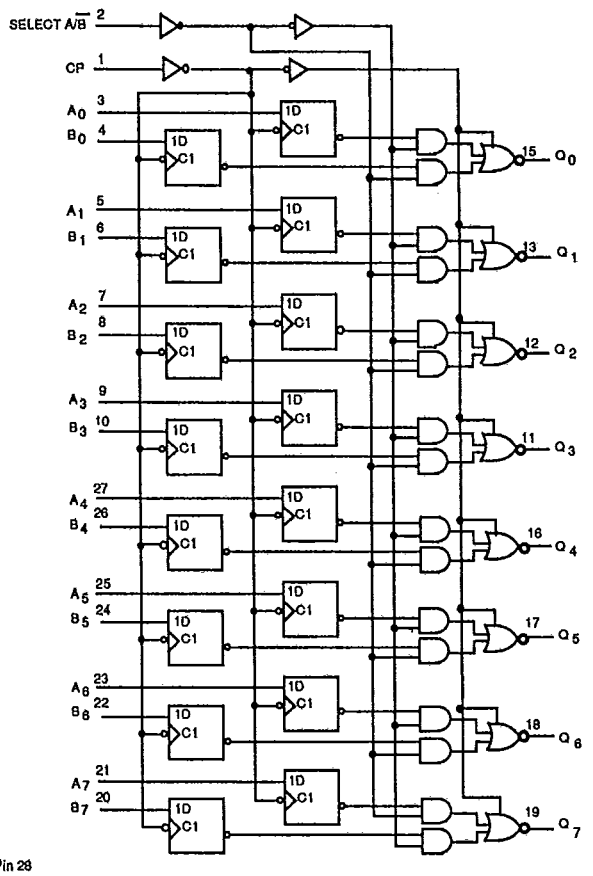
LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	CP	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	OFF
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = High voltage level
L = Low voltage level
X = Don't care
OFF= Pulled up through resistor (open collector)
↑ =Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=4.5V					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX	A_n = B_n = SELECT A/$\overline{B}$ = 4.5V, CP =↕			80	100	mA
		I_{CCL}		A_n = B_n = SELECT A/$\overline{B}$ = GND, CP =↕			85	105	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

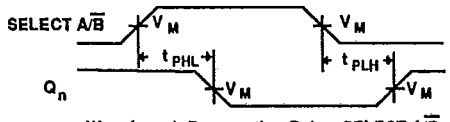
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B register)	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A register)	Waveform 1	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 3	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

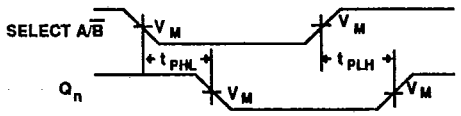
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	1.0 3.0			2.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	1.0 2.0			2.0 3.0		ns
$t_w(H)$	CP Pulse width, High	Waveform 4	5.0			6.0		ns

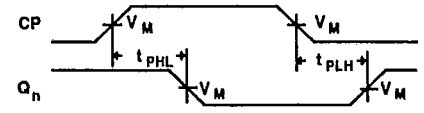
AC WAVEFORMS



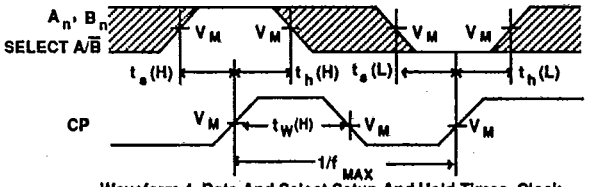
Waveform 1. Propagation Delay, SELECT A/$\overline{B}$ To Output (A register stored data=Low. CP=H)



Waveform 2. Propagation Delay, SELECT A/$\overline{B}$ To Output (B register stored data=Low. CP=H)



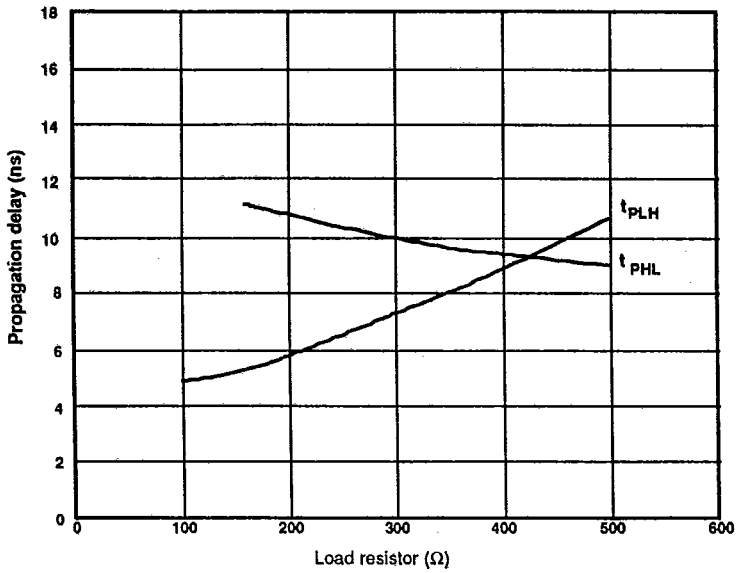
Waveform 3. Propagation Delay, Clock To Output (A register stored data=Low. SELECT A/$\overline{B}$=H,)



Waveform 4. Data And Select Setup And Hold Times ,Clock pulse width , And Maximum Clock Frequency

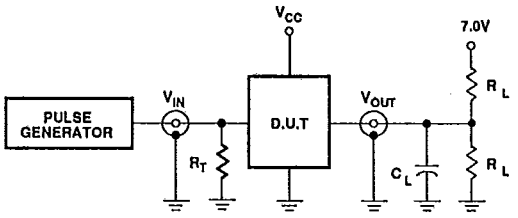
NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

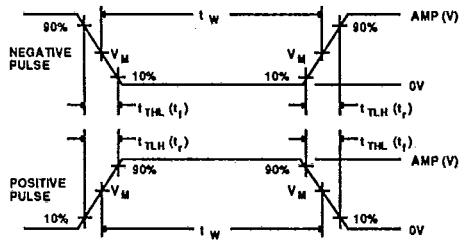


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns